data from texture palette 650 to generate an output pixel for a new video frame. Mapping address generator 615 provides fractional pixel positioning information to bilinear filter 625.

B6 cont. *Please replace the paragraph beginning on page 16, line 14 with:*

Multiple GFXBLOCK commands can exist in the pipeline of Figure 6 simultaneously. As a result correction data streams through texture palette 650. Read and write accesses to texture palette 650 are managed such that the correction data streams do not overwrite valid data stored in the texture palette 650.

IN THE DRAWINGS

Figure 5 has been amended to reflect a grammatical correction, and to maintain consistency with the specification. Specifically the label "Chromanance" was changed to "Chrominance" in two blocks of Figure 5.

IN THE CLAIMS

1. (Amended) A method of motion compensation of digital video data, the method comprising:

receiving a motion compensation command having associated correction data related to a macroblock;

B7 storing the correction data related to a macroblock in a memory according to a first order corresponding to the motion compensation command;

performing frame prediction operations in response to the motion compensation command;

reading the correction data related to a macroblock from the memory according to a second order; and

combining the correction data related to a macroblock with results from the frame prediction operations to generate an output video frame.

6. (Amended) An apparatus for motion compensation of digital video data, the apparatus comprising:

means for receiving a motion compensation command having associated correction data related to a macroblock;

means for storing the correction data related to a macroblock in a memory according to a first order corresponding to the motion compensation command;

means for performing frame prediction operations in response to the motion compensation command;

means for reading the correction data related to a macroblock from the memory according to a second order; and

means for combining the correction data related to a macroblock with results from the frame prediction operation to generate an output video frame.

11. (Amended) A circuit for generating motion compensated video, the circuit comprising:

a command stream controller coupled to receive an instruction to manipulate motion compensated video data;

a write address generator coupled to the command stream controller;

a memory coupled to the command stream controller and to the write address generator, the memory to store pixel data related to a macroblock in a first order determined by the write address generator;

processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame; and

a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output the pixel data related to a macroblock in a second order.

14. (Amended) A circuit for generating motion compensated video, the circuit comprising:

a command stream controller coupled to receive an instruction to manipulate motion compensated video data;

a write address generator coupled to the command stream controller;

a memory coupled to the command stream controller and to the write address generator, the memory to store pixel data in a first order determined by the write address generator;

processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame; and

a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output pixel data in sub-block-by-sub-block row major order.

17. (New) The method of claim 1 wherein the second order is based on row major order.

18. (New) The apparatus of claim 6 wherein the second order is based on row major order.

19. (New) The circuit of claim 14 wherein the circuit is pipelined.

20. (New) An apparatus comprising:

a command stream controller coupled to receive an instruction to manipulate motion compensation video data;

a memory coupled to the command stream controller, the memory to store pixel data related to a macroblock in a first order;

a read address generator coupled to the memory, the read address generator to cause the memory to output the pixel data related to a macroblock in a second order; and

a processing unit coupled to the read address generator and to the command stream controller, the processing unit to perform motion compensation operations and texture mapping operations utilizing common circuitry.

21. (New) The apparatus of claim 20 wherein the first order is based on output from an Inverse Discrete Cosine Transform (IDCT) operation and the second order is based on row major order.

22. (New) The apparatus of claim 20 wherein the processing unit further comprises:

a memory to store reference pixels;

a mapping address generator to provide read addresses for the reference pixels;

a bilinear filter coupled to the memory, the bilinear filter to access the reference pixels from the memory and to filter the reference pixels; and